

FIG. 1

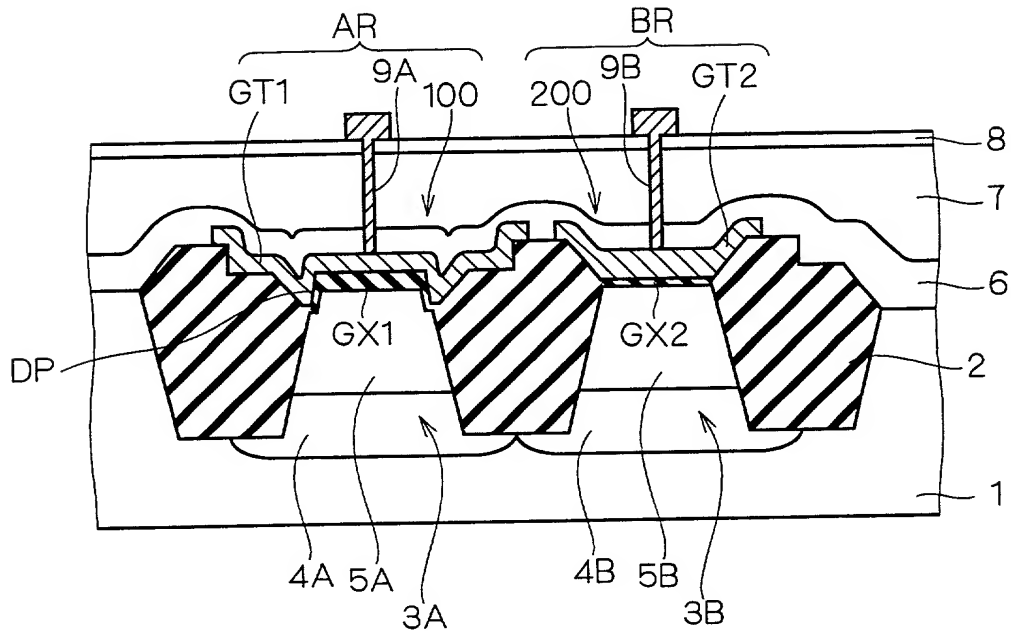


FIG. 2

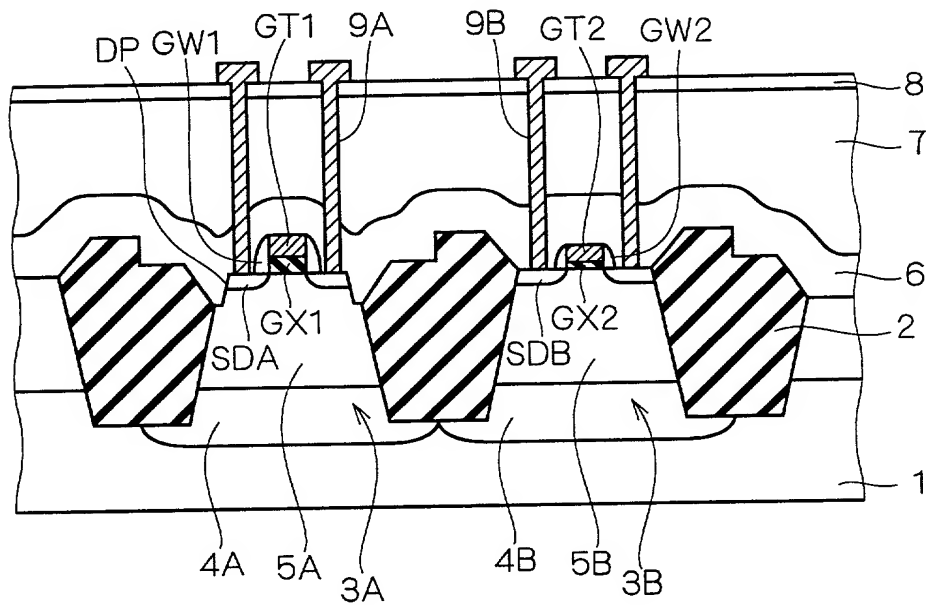


FIG. 3

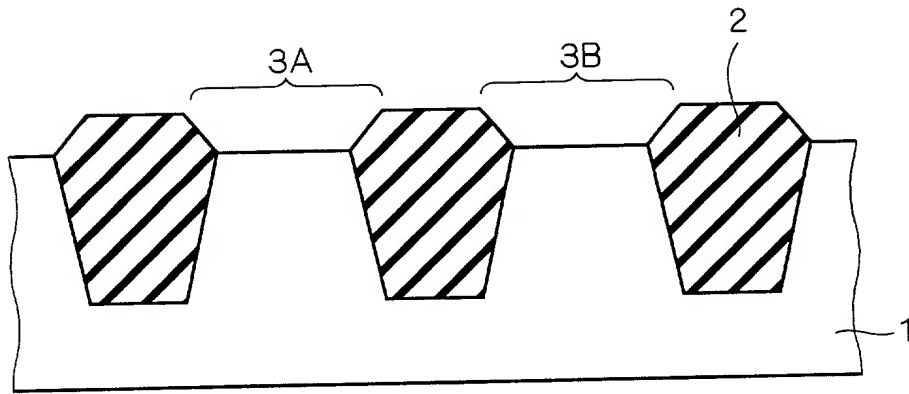


FIG. 4

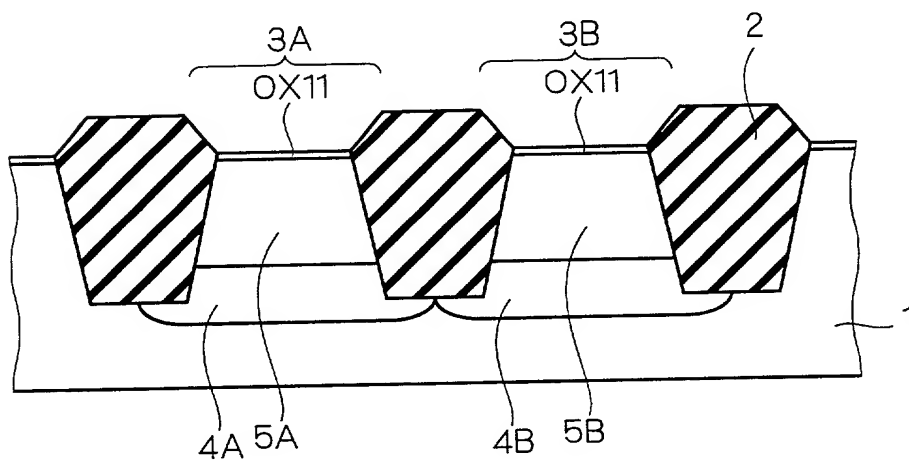


FIG. 5

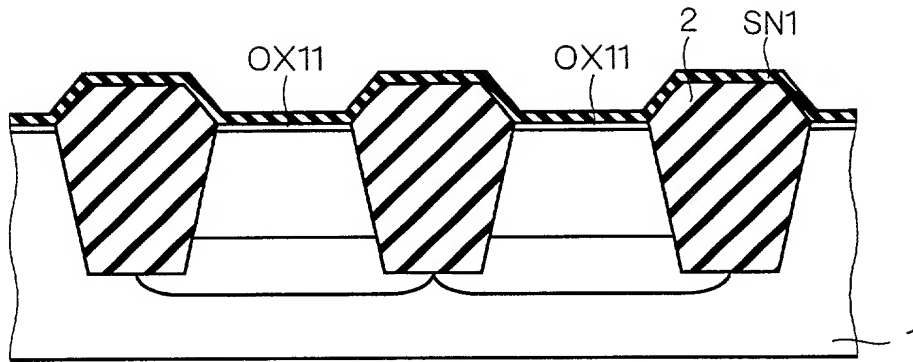


FIG. 6

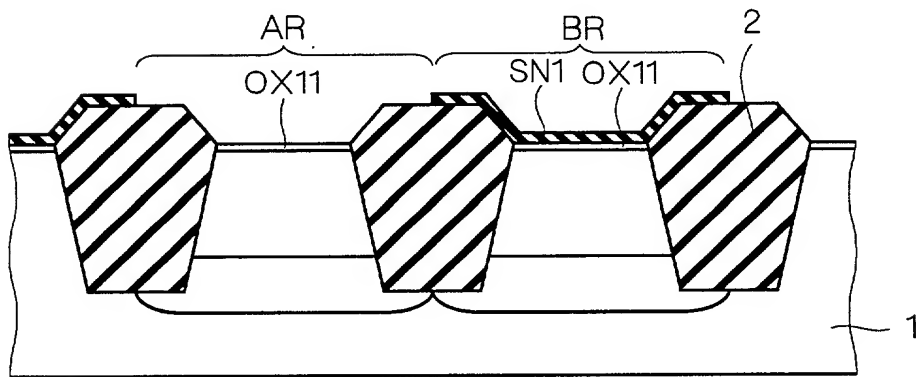


FIG. 7

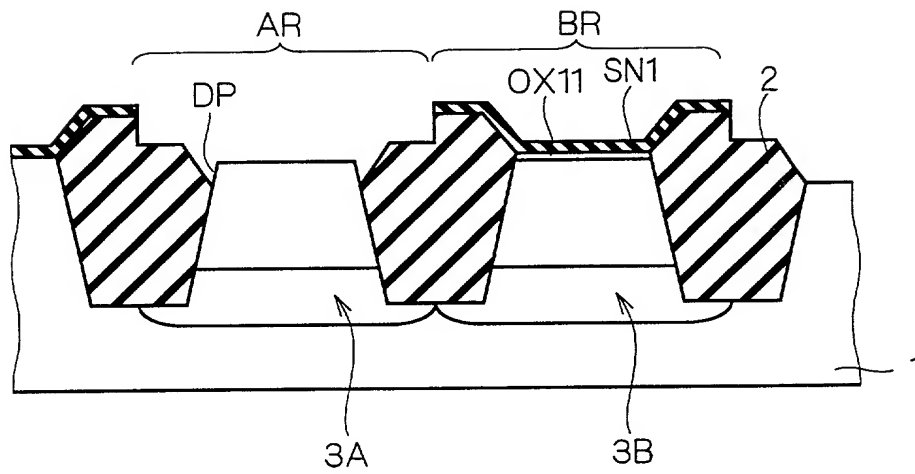
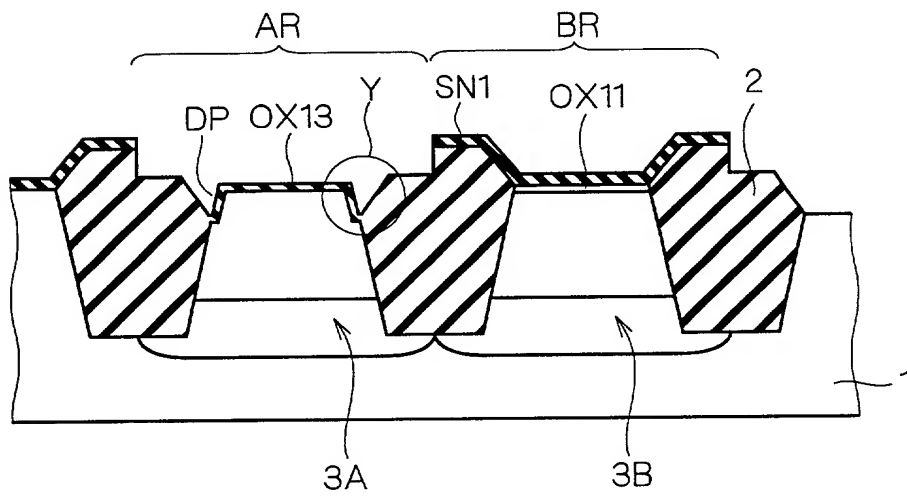
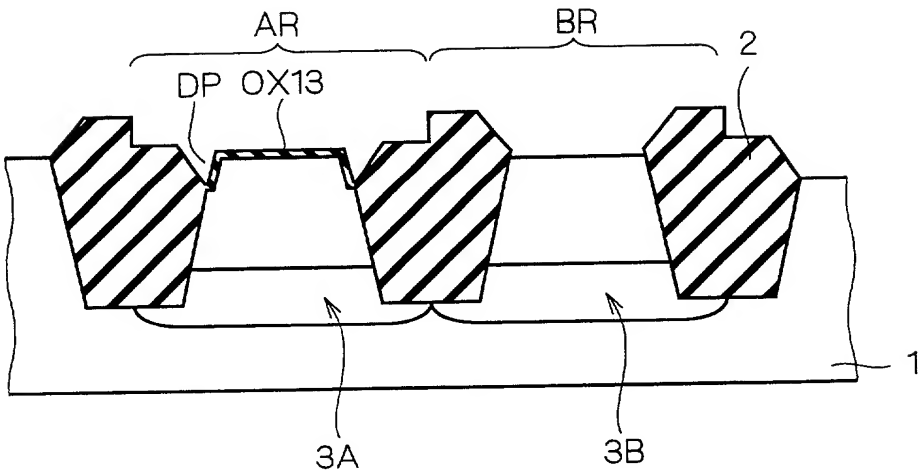


FIG. 8



F I G . 9



F I G . 10

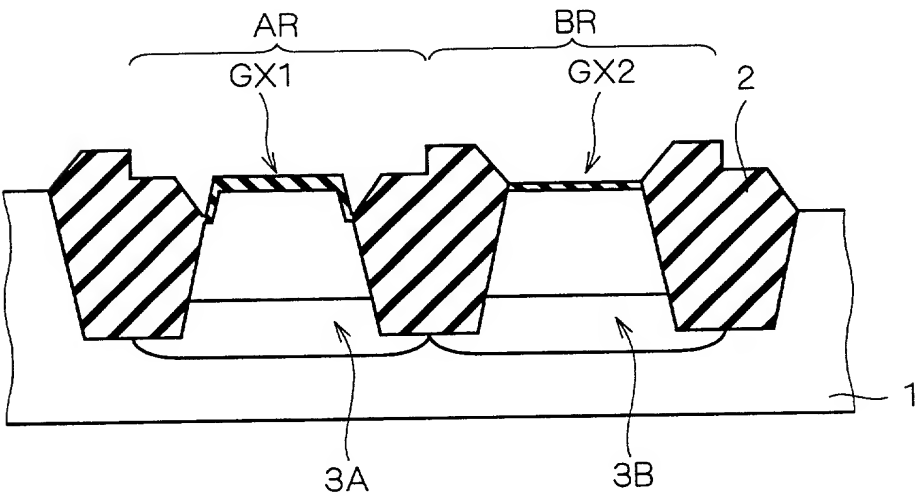


FIG. 11

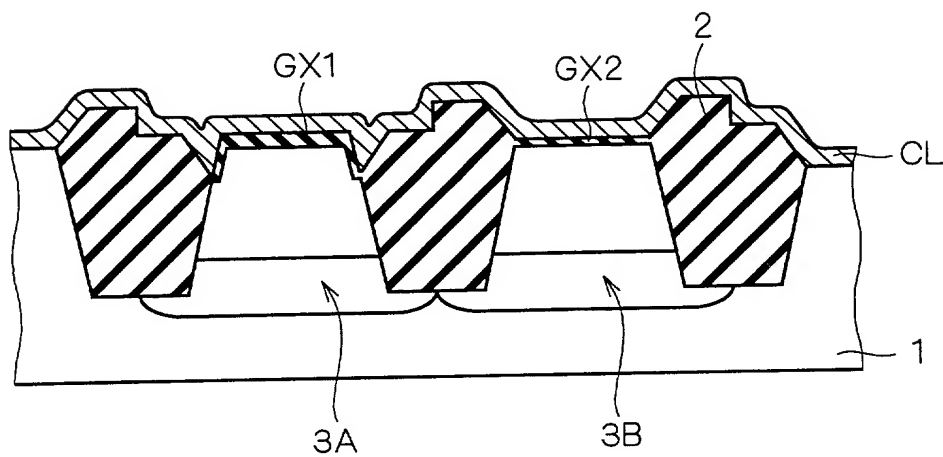
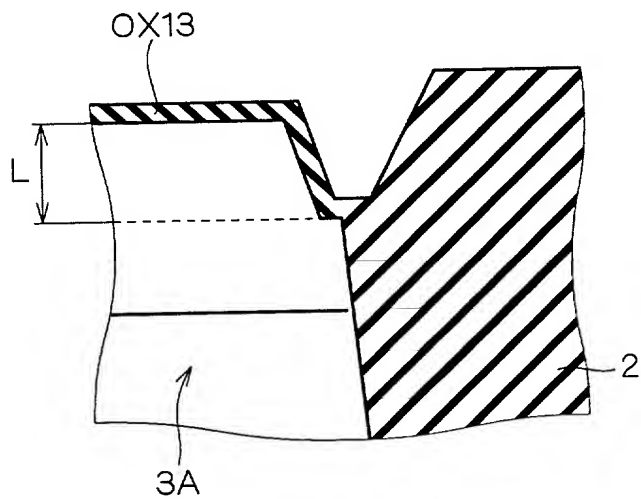


FIG. 12



THRESHOLD VOLTAGE [V]

Q

0.2 ~ 0.3V

AREA D1

10

AREA D2

P

0

DEPTH OF RECESS AROUND ACTIVE REGION (nm)

[illegible]

FIG. 16

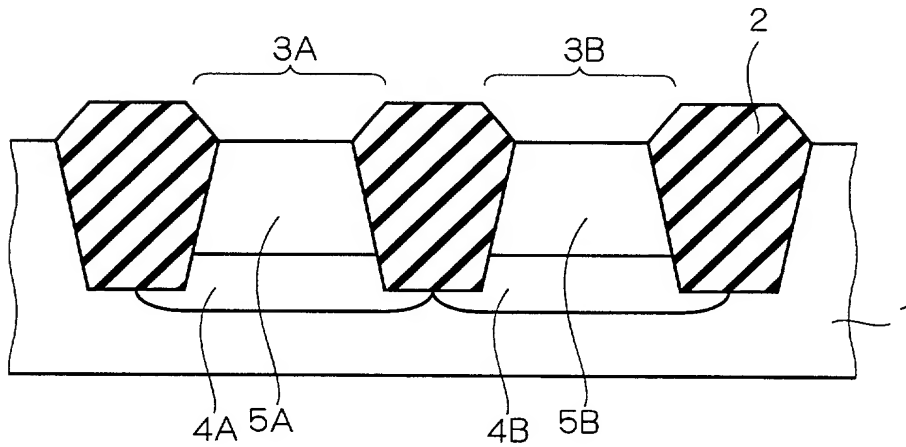




FIG. 17

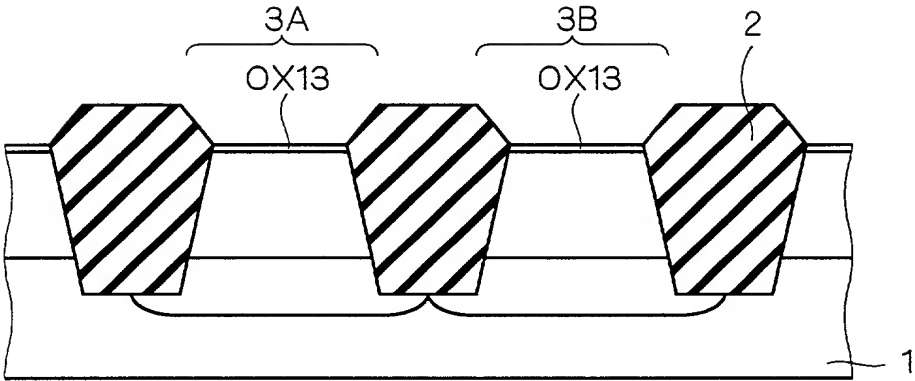
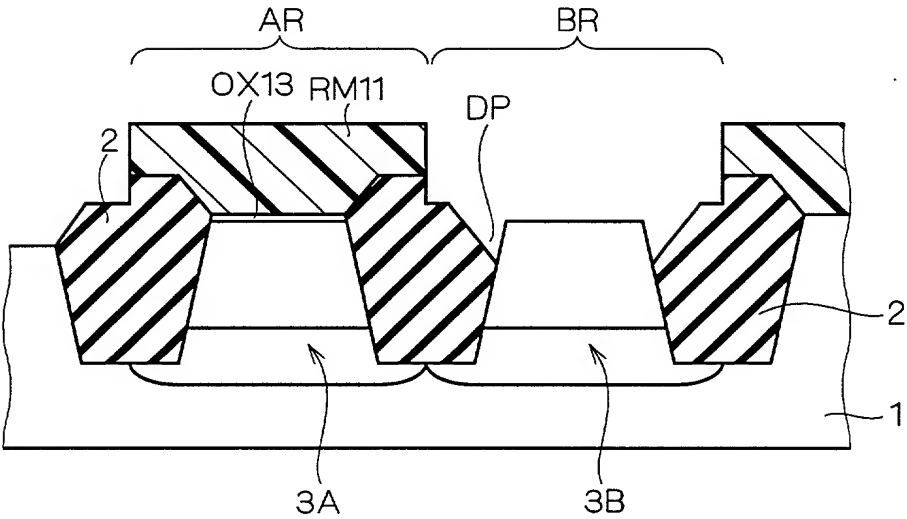
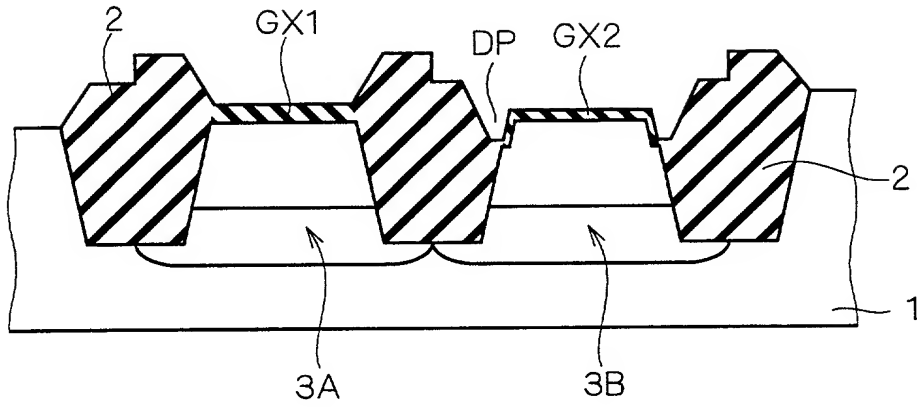


FIG. 18



F I G . 1 9



F I G . 2 0

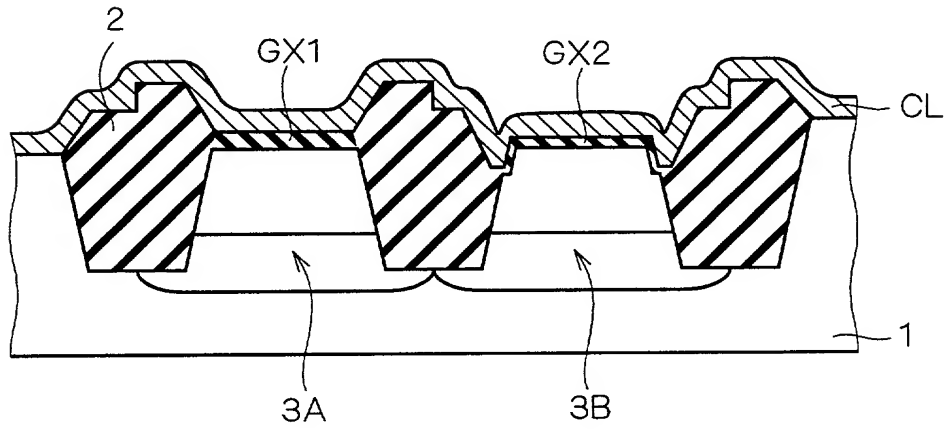


FIG. 21

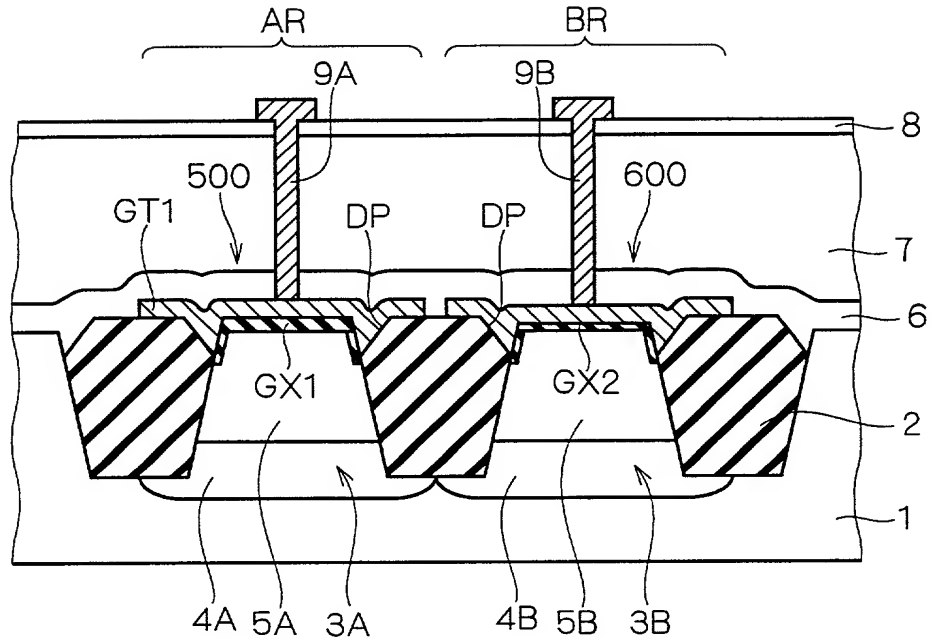


FIG. 22

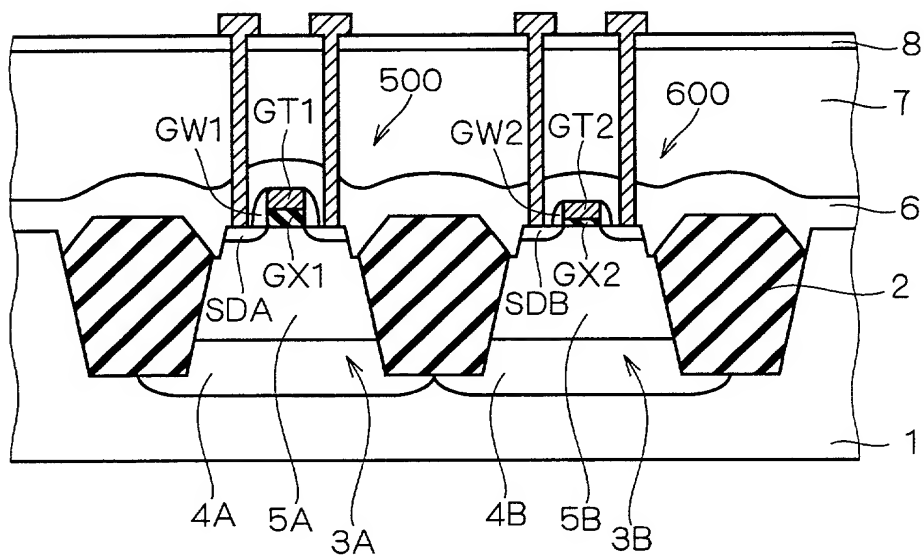


FIG. 23

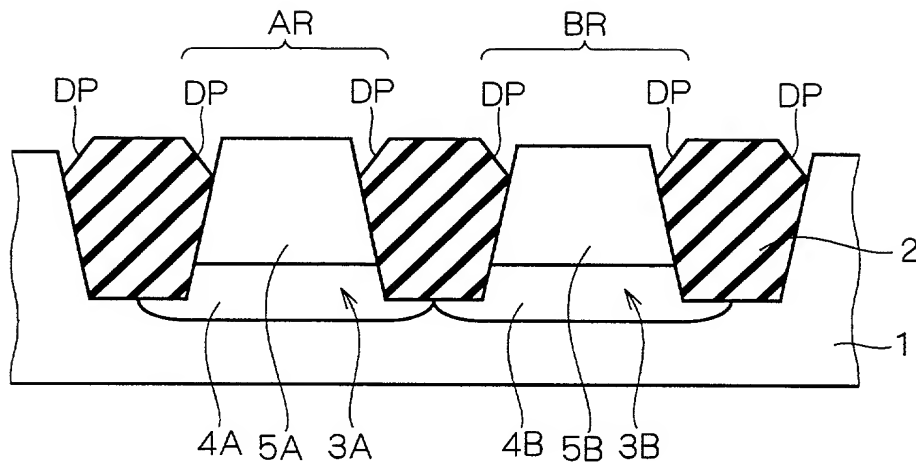
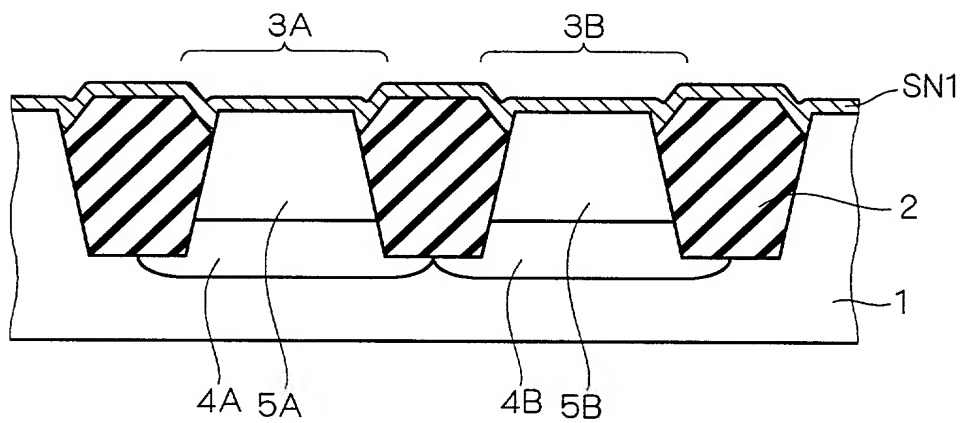
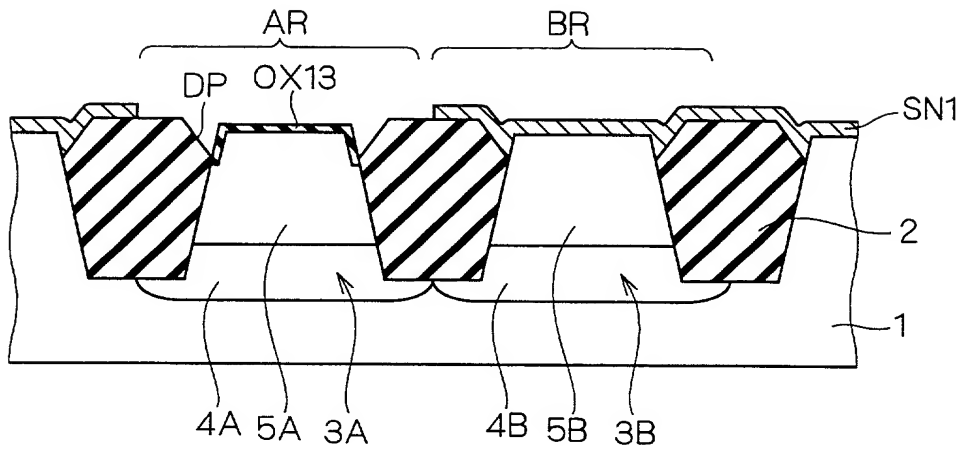


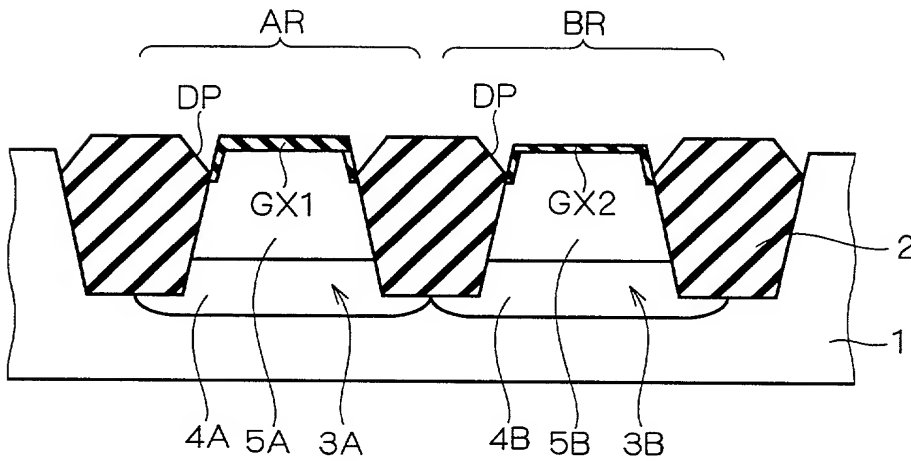
FIG. 24



F I G . 2 5



F I G . 2 6



A cross-sectional view of a semiconductor device. A substrate 1 is shown at the bottom. On top of the substrate, there is a layer 2. This layer 2 has a series of rectangular openings. The first opening is labeled GX1 and the second is labeled GX2. The layer 2 is formed on a base layer 3A and 3B. The top surface of the layer 2 is labeled CL.

A detailed cross-sectional view of a semiconductor device. The device is built on a substrate 1. Two gate regions, AR and BR, are defined by gate electrodes GT1 and GT2. Between these gates are regions 4A and 4B, which are part of a larger structure 2. Above the gates are layers 9A and 9B, which are part of a larger structure 10. A central region DP is located between the gates. The device also includes layers 3A and 3B, and a top layer 8. Other labels include 5A, 5B, 6, 7, and 1.



FIG. 31 (BACKGROUND ART)

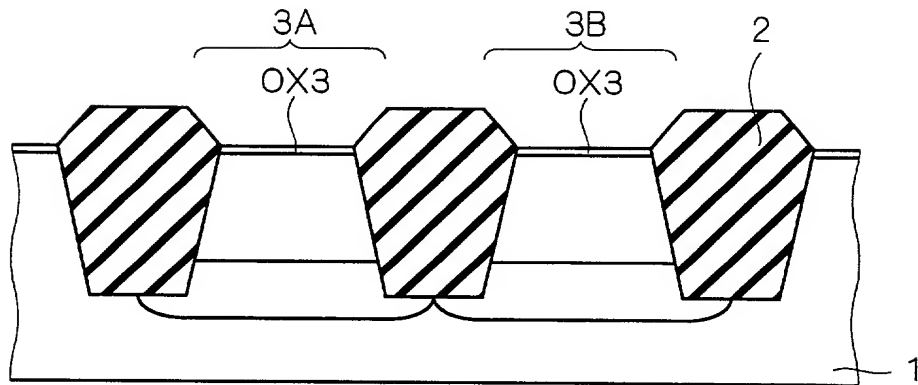


FIG. 32 (BACKGROUND ART)

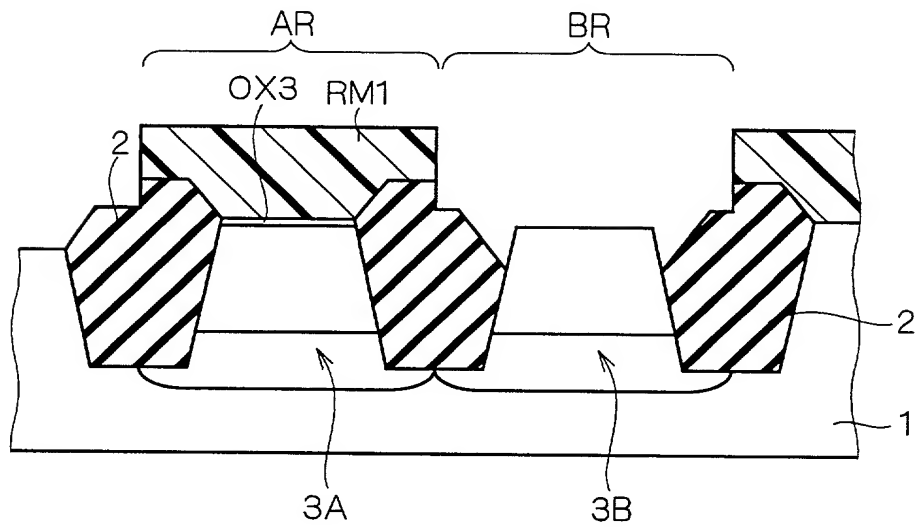




FIG. 33 (BACKGROUND ART)

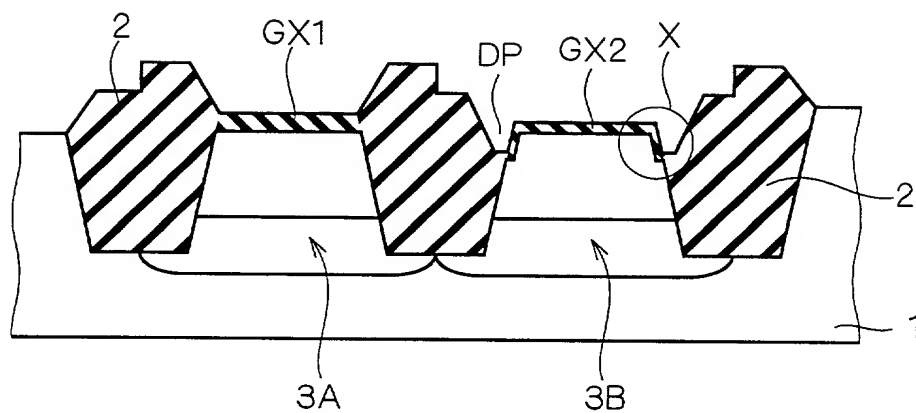


FIG. 34 (BACKGROUND ART)

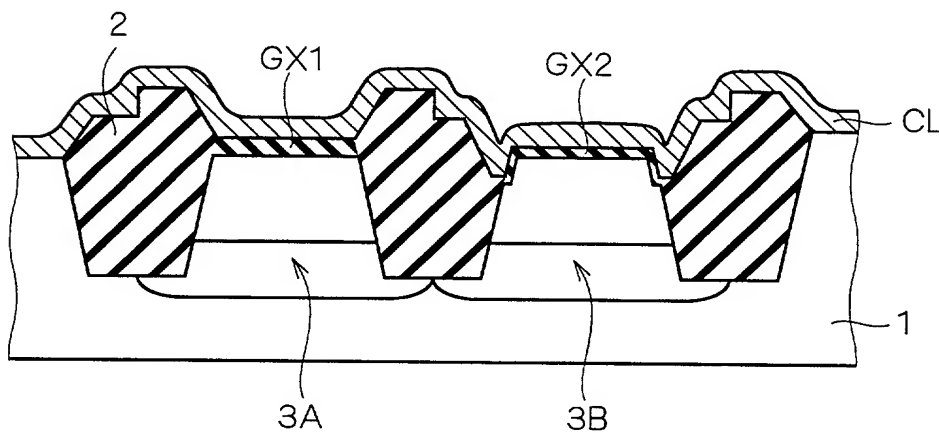


FIG. 35 (BACKGROUND ART)

